A NETWORK TIMING CONCEPT FOR SWITZERLAND

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ABSTRACT

Studies on network timing started in Switzerland in 1974, preparing the future conversion to digital transmission and switching, stimulated by the development of integrated electronics. First generation equipment was specified and developed in 1975/76, when early international standards recommending 10^{-11} long term stability were drafted. Further work led to the present network timing concept in which the network is divided into 3 regions, each cesium-controlled in a preselected master-slave mode with 4 levels of hierarchy. All major (2nd order) nodes are served by triple-redundant, microprocessor-controlled precision crystal oscillators. The third order level is constituted by the digital switching centers.

1. INTRODUCTION

The operation of a digital communications network is characterized by time-multiplexed transmission and switching. The various operations on the flow of digital information depend on proper timing of all events in order to minimize errors.

Historically, digital transmission is older than digital switching. It started here in Switzerland 15 years ago with the introduction of pulse code modulation (PCM) transmission systems on existing symmetric pair lines in the rural network in order to increase their telephone traffic capacity. These systems worked in an analog environment, combining 30, 64 kbit/s channels in a PCM frame with additional 2 channels for frame identification and signalling, resulting in a standardized 2048 kbit/s PCM-signal. This operation is known as time division multiplexing (TDM) since each channel in a frame occupies a definite time slot carrying an 8 bit word. At the receiving end, the signal is demultiplexed and decoded to reconstruct the 30 analog voice channels. In the coders and the multiplexers, all digital operations on the signals are controlled by a clock oscillator. The demultiplexing requires the same clock signal exactly at the same rate. Furthermore, the start of the frame must be identified.

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Such a digital transmission system can thus operate only if the bit as well as the frame times are correctly defined, i.e. it requires bit and frame synchronization. The bit synchronization is the more fundamental operation since if it is maintainted, then the frame synchronization is obtained by digital logic operations controlled by the bit synchronous clock signal. The subject of this paper therefore deals only with the aspects of bit synchronization and timing.

We use the term "network timing" instead of synchronization because of the meaning the term synchronization has been given to in the literature. Most authors use it for designing the acquisition and tracking of a receiver clock on some information contained in the received signal. In our context, network timing has a more general meaning, i.e. establishing and maintaining timing and frequency control of all clocks throughout an extended network with the accuracy and reliability required for operation at all levels. This, of course, also implies synchronization in the narrower sense mentioned above.

The first 2048 kbit/s PCM links installed for cable transmission in an analog environment did not require external timing control and operated well within an easily achievable frequency accuracy of ± 50 ppm, since no interaction was taking place with other digital systems. The question of timing control only arises if there are several sources of digital information (generated by clocks in every source) to be processed in multiplexing, transmission and switching systems.

To illustrate the problem, we mention the 30 channel synchronous 64 kbit/s - 2048 kbit/s multiplexer described in more detail in the reference [1]. Each 64 kbit/s bit stream generated by its own independent clock is written into a buffer memory. The common clock of the multiplexer reads the information out at its higher 2048 kbit/s rate, 8-bit words at a time. Depending on the average rate difference between the clocks, it may occur that an 8-bit word is either read twice or not at all (buffer overflow, i.e. data loss). Such an event is called a slip and always constitutes a temporary corruption of the transmitted digital data stream. In general, the timing variations show systematic and random behaviour. The average slip frequency is a statistical quantity and depends on the timing variations as well as on the buffer size.

Digitally encoded voice at the standard 64 kbit/s PCM bit rate is relatively tolerant to slips as only about every 25th 8-bit word (octet) slip causes an audible click. Data transmission between computers is obviously less tolerant, even taking into account the available means of error detection and correction by appropriate coding which reduce the link throughput and introduce additional delay.

In the early seventies, the accelerating pace in the development of digital electronics opened the way towards the establishment of entirely digital networks. Integration, first of transmission and switching (Integrated Digital Network, IDN) and then of services (Integrated Services Digital Network, ISDN) became recognized as being the concepts of the future. New transmission media such as satellites and optical fibers are offering increased capacity at lower

cost, being welcome for accommodating the growing demand, especially in data communications. Worldwide communications require technical standards, recommended by the competent consultative bodies of the International Telecommunications Union, i.e. the CCITT Study Group XVIII for digital networks and CCIR for radio communications. Recommended standards for network timing are part of the performance objectives for digital networks, especially in the CCITT Recommendations series G. 800.

This paper reports on work performed in Switzerland during the last ten years. In Section 2, the elements of timing network design are discussed with regard to the modeling of parameters, their interactions and the options chosen during the evolution of the project. Section 3 presents the present status of the concept which now is in course of implementation.

Additional information about the current state of digital network timing planning has been presented and discussed in Ref. [9].

2. ELEMENTS OF TIMING NETWORK DESIGN

2.1 Clocks

In the context of this paper we use the term "clock" to designate the equipment which generates the timing signals at all nodes of the network. These clocks thus determine the bit rates at which the digital information is generated, multiplexed, and processed in the switching centers.

The main design parameters entering in the clock unit's specifications are:

- accuracy and stability of the clock frequency.

- reliability of the clock unit, i.e. availability of the output signal.

The reliability is most important as the failure of the clock in a digital processing equipment causes a total failure of all its functions.

The accuracy of the clock's frequency is characterized by the uncertainty of its setting with respect to the legal unit, i.e. the second or its inverse, the Hertz.

The clock's output signal is usually a sinusoidal voltage, from which square waves or pulse trains are derived. Their step transitions can be related within a small fraction of the period to the zero crossings of the clock output signal. The timing transitions of any real clock show a cumulative growing departure from a strictly periodic timing sequence assumed as an ideal reference, i.e. the timing error of any real clock increases with time without bounds.

Clock frequency instability is to be characterized considering systematic as well as random departures from the nominal value. Systematic effects include the already mentioned setting uncertainty, long term drift and, to some extent, known environmental influences such as cyclic temperature variations. Random effects are characterized by statistical modeling which allows to predict the probable departure of frequency and time from the nominal value. If the time differences between the clocks in a network exceed the limits set by the buffer memory capacity, slips will occur. After a slip, the memory is set to an intermediate value and it starts to be filled or emptied again until the next slip occurs. This "controlled slip" operation is equivalent to resetting the clock's time. It is in principle possible to operate a network with free running clocks at all nodes, provided these clocks have sufficient accuracy and stability in order to limit the statistical frequency of slips. This mode of operation is called plesiochronous (from greek plesios = near, i.e. nearly on time). It requires only minimum network management, i.e. only infrequent frequency adjustment of some of the clocks, if the latter are of high accuracy and stability such as cesium clocks [1]. However, high stability clocks are more complex, thus less reliable and more expensive than simple crystal oscillators. Well designed crystal oscillators have low phase noise and excellent short term stability. Temperature controlled ovens allow to reduce the effects of ambient temperature variations to a low level. Frequency drift due to aging of the crystal resonator and its associated circuits is the main problem to be handled by means of automatic frequency control on an external reference.

The task of designing optimal frequency control systems where the external reference signal is transmitted over a communications link is of such importance in the field of synchronization that it has been treated in a vast amount of literature during the last twenty years. The basic control device is the phase lock loop (PLL). The frequency of the oscillator is controlled by a voltage proportional to the phase or time difference between its output signal and the reference signal. Phase is the time integral of angular frequency, thus in a stable PLL, the long term frequency difference between the reference and the controlled clock tends towards zero. Designing optimum PLL circuits requires the knowledge not only of the clock oscillator's parameters, but also that of the reference signal under all conditions of operation. A severe fault to be avoided by all means is the phenomenon of cycle slipping in which the control loop temporarily loses its lock and the clock loses or gains one or several cycles so that its timing properties become erratic and unpredictable.

In the present design, the properties of the digital frequency control loop, the associated monitoring circuits and the choice of crystal oscillators having high stability in the free running mode contribute towards negligible probability of cycle slipping.

Requirements for new design of clock units for the Swiss PTT network appeared around 1973. Experience on the use of stable oscillators in the transmission network existed then for over 20 years, as carrier generator equipment used for frequency division multiplex (FDM) systems in the coaxial cable and microwave relay trunk line network. Growing demand for transmission capacity for

telephone traffic and for data transmission on leased lines, the need for re-
placement of obsolete equipment and the plans for conversion of the network to
digital transmission and switching were the driving forces for the development
of new carrier generator and clock equipment. Tentative specifications were
established in 1974, design and development started in 1975 and was completed
in 1977. Two sets of performance specifications had to be established. For an-
alog FDM carriers, the accuracy had to be better than 2 parts in 10^8. A rather
stringent requirement was that for the carrier phase noise: sideband power
spectral density had to be less than -120 dB per Hertz below the carrier in
the range 50...4000 Hz offset from the carrier [3]. For digital transmission
application as a master center, the accuracy and long term stability was re-
quired to be better than 1 part in 10^{11} in order to fulfill the CCITT Recom-
mendation G. 811 issued in 1976. A discussion of these requirements has been
published in 1977 [4] as well as a description of the equipment [5]. The main
features of this equipment were:

- two 5 MHz oven-controlled crystal master oscillators

- optional cesium primary master

- twin 5 MHz master buses, each feeding the 2 redundant sets of output signal
  synthesizer generators

- twin redundant power supply system

- surveillance and alarm circuits according to established transmission line
  equipment standards

- mechanical design according to Swiss PTT Standard Equipment Practice BW72
  for transmission line equipment.

Beginning in 1978, these standard clock units were installed in the trunk net-
work. In the digital data part of the network there are currently 14 units ha-
ving the cesium master in operation.

2.2 Links

As mentioned in the preceding section, the design of an automatic clock fre-
quency control system in which the reference signal is generated at a distant
node and transmitted over a link requires the knowledge of this reference sig-
nal's characteristics. Any transmission system introduces a delay and varia-
tions of this delay appear at the output of the link as variations in the ti-
ming of the signal in addition to the timing variation of the clock generating
the signal at the other end. We can measure and analyse the frequency and ti-
ming instabilities of the received signal but there it is not possible to se-
parate the two contributing parts, i.e. clock variations and delay variations,
if both are of the same order of magnitude. In the literature published until
about ten years ago, almost nothing could be found on measurements of signal
delay, whereas theoretical work on network synchronization was abundant (see
list of references in [1]). For reasons of flexibility in network management
and to facilitate network growth, it was decided at the beginning to attempt
using the timing information contained in the basic 2048 kbit/s first order

PCM multiplex as reference signal, i.e. to avoid the design and construction of dedicated synchronization links.

Therefore, the properties of delay variations on this type of signal had to be determined. Two main types of delay variations are the most important:
- jitter
- wander

The term "jitter" designates rapid variations of the times at which the transitions between the logic states in the signal occur, i.e. variations around a mean value averaged over a few seconds.

The term "wander" designates slow variations of this mean value. Both jitter and wander have known causes: The two main contributors to jitter are variations of the logic transition thresholds depending on the bit pattern which occur in regenerative repeaters inserted in long transmission lines and waiting time jitter generated in higher order multiplexers using bit stuffing. The highest peak-to-peak jitter amplitudes observed are of the order of a few hundred nanoseconds. The jitter spectrum is approximately flat up to a cutoff frequency which depends on the transmission systems parameters and exceeds 1 kHz only in rare cases. Above the cutoff it decreases with a slope of at least 20 dB/decade.

The main cause of wander in the transmission link is the dependence of delay on the temperature. The temperature coefficients of standard size coaxial cables and optical fibers are known to be less than 0.1 nanoseconds per kilometer and degree centigrade. The influence of temperature on line equipment usually plays a lesser role. Step changes of the delay occur through switching between different line sections which are relatively infrequent and usually related to defects accompanied by signal interruptions. Transient effects due to electromagnetic interference must also be taken into account.

2.3 Network operation modes

During the development of network timing concepts, two main principles of operation modes for the clock control have been discussed [1, 4]
- mutual synchronization
- master-slave synchronization.

The mutual synchronization method could be called "democratic" since it is based on mutual control of all oscillators having the same rank in the network, each taking its reference from the average of a number of incoming signals. The master-slave method is hierarchical, i.e. there is a master clock which controls other clocks of lower rank.

From the viewpoint of network topology, mutual control appears to be best fit for meshed networks, whereas tree- and star-like networks are hierarchical in their general organization and therefore better suited for master-slave operation.

2.4 Design options and choices

During the development of the network timing concept some choices between design options mentioned in the preceding sections had to be made. The criteria for these choices included the present and projected requirements for the digital network, requirements for existing analog transmission systems, minimum overhead for network management, operational experience with earlier and existing equipment and economic aspects. The small team working on this project comprised engineers from the R & D, transmission engineering and operating divisions of the Swiss PTT, allowing early and continuous input on matters of planning, operation and maintenance. The two most important choices made during this project were:

a) the use of standard 2048 kbit/s PCM links (CCITT Recommendations Series G. 700) to transmit the reference signals to controlled clocks. This choice allows the highest flexibility for the network configuration and high transmission reliability through redundancy of links at no additional cost.

b) the choice to operate the timing network in the master-slave mode. The national network is subdivided into three regions, each with a cesium-controlled master, i.e. the regional networks are plesiochronous (CCITT Rec. G. 811).

A guideline based on the general policy of the Swiss PTT was to keep in pace with the work on international standards in CCITT Study Group XVIII (Digital Networks), CEPT (Conférence Européenne des Postes et Télécommunications) and the CCIR Study Group 7 (Standard Frequencies and Time Signals). These standards published in the form of recommendations establishing minimum performance limits and interface specifications constitute the basis for the operation of networks on the international level but leave considerable freedom for the actual system and equipment design.

The decision to operate in the master-slave mode was taken in 1979 after careful studies of all aspects involved [1]. The structure of the present network with its projected traffic carrying capacity extensions is hierarchical. Using a stochastic network model it has been shown, that the required reliability can be obtained with a minimum of network management overhead. The impact of network extensions introducing new links and switching centers remains confined to the affected part of the network and has no influence on the parameters governing control stability in other parts of the network. Especially, disturbances in clock control will affect only a restricted region, avoiding the risk of propagating an instability into other regions.

The subdivision of the network into three regions, each having a cesium-controlled master, allows to keep the peak-to-peak wander well below the storage buffer capacity. The three regions operate in the plesiochronous mode. In case of failure of a regional master, the region is automatically slaved to one of the other masters. There is another fundamental reason to the choice of the number three of masters: three is the minimum number of clocks allowing an

early detection of a fault by comparison and majority decision. As described in section 3, this principle has also been applied at the next lower level, i.e. the second level of hierarchy.

The studies which have led to the decision in favor of the master-slave mode did also take advantage from the greater transparency and simplicity of its design compared to that of mutual control systems. An illustrative analysis of the control chain composed of master, PCM link and slave oscillator has been made and published in 1980 [6]. It is based on the statistical clock model of CCIR Recommendation 538, the same line jitter model as that used in Ref. [1] and real data on cesium-standards and various commercial types of crystal oscillators, including a new original development using BVA-type electrodeless quartz crystal resonators having an aging rate of less than 10^{-11}/day [7]. Low aging rates of this order of magnitude allow to increase the remote frequency control loop time constant to a few thousand seconds. Then, the filtering properties of the PLL reduce the effect of PCM line jitter to negligible values.

Step frequency control of the slave oscillators was already used in the 1977 generation clock units [7]. This method allows blocking of the frequency control servo during interruptions of the reference signal, leaving the slave oscillator free running on the last known good setting until restoration of the reference.

However, as there were only two oscillators in this earlier equipment, some oscillator failures could not be unambigously detected without having recourse to an external known good reference. It was therefore decided to specify a secondary level master clock unit with three oscillators, each having its PLL control loop with memory and three redundant reference signal lines.

The PLL units described in more detail in Ref. [8] are of recent design. The main features are determined by the software of the microprocessor control system. It is thus possible to adapt the control system parameters such as step size, alarm criteria and time constant to the operational conditions encountered in the network without hardware changes. Another example of a microprocessor controlled PLL, except for associated monitoring and alarm circuitry, is described in Ref. [10].

A surveillance unit with majority decision allows to identify a clock showing excessive drift quickly and locally, i.e. without having recourse to the jitter impaired external references. This configuration allows full compliance within a comfortable margin with the current CCITT recommendations. Compared to the cost of a complete clock bay, the additional expense is a modest percentage compared to a high gain in operational reliability.

3. THE PRESENT NETWORK TIMING CONCEPT

3.1 Timing network structure

The timing network structure is shown in Fig. 1. The cesium-controlled master centers constitute the highest, first order of the hierarchy. The network is subdivided into three timing regions of about equal importance. There are currently over one million telephone subscribers and a growing proportion of customers requiring data communications in each region. The first order centers are placed in nodes offering the highest number of direct links to the second order centers. The first and second order centers are connected through the long distance trunk line network. The links are constituted of 2.6/9.5 mm and 1.2/4.4 mm coaxial cable, radio relay and optical fiber systems, operating on higher order multiplex bit rates of 140 and 565 Mbit/s. Radio links operate on 34 or 140 Mbit/s. The long distance network has a meshed structure, but the timing links are selected to form a tree structure as shown in the figure. There are no more than 2 second order centers in cascade. Each second order center receives its reference signals over three redundant links chosen to be as separate as possible, except during buildup, when only two or one cable or radio link will be available. With this hierarchical structure, the timing network will grow at the same pace as the digital transmission network itself. The lower order centers are connected through the district and local networks.

3.2 First order centers

Fig. 2 shows schematically the principal elements of a first order center. It differs from the second order centers only by the configuration of the master oscillators which, in this case, comprise one cesium controlled oscillator and two PLL-units with a BVA crystal controlled oscillator. The 5 MHz output signal of the cesium master in split and then separately combined with the outputs of each PLL on two 5 MHz bus units. The 5 MHz PLL output signals are each attenuated by 6 dB (one-half amplitude) before vector addition to the master signal. Any phase relationship is thus allowed between the two components, cancellation during 180 degree opposition being prevented. Amplitude variations are suppressed in the bus unit by means of a limiter. The two PLL-units A and C are each slaved to a reference signal transmitted from the two other first order masters. Slow phase variations on the vector sum, due to wander and systematic frequency differences are limited to 33 ns peak-to-peak, negligible for the network operation.

The reference signals are tapped from 2048 kbit/s PCM signals by means of a timing extraction unit (TEX) which generates a 2048 kHz sine wave and also contains an Alarm Indicator Signal (AIS) detector which indicates faults in the PCM transmission system. Supervision and alarm systems as well as the output circuits connected to the twin 5 MHz buses are the same in the first and second order centers.

In case of failure of the cesium unit, which has a MTBF of 3,5 years (CCIR Report 898), its supervised output is cut from the bus. The PLL's A and B then

continue feeding the twin buses, each PLL remaining slaved to one of the other two first order centers. If all three cesium masters should fail simultaneously, the three first order centers fall back into a mutual control mode. A third, spare reference line can be manually plugged to the PLL units during emergency.

3.3 Second order centers

As shown in the block diagram of Fig. 3, the structure of the second order centers is similar to that of the first order centers. The main difference is the presence of 3 PLL-units A, B and C instead of a cesium master in the position B. The three PLL-units each receive a 2048 kHz reference from a TEX unit connected to a separate 2048 kbit/s PCM line, originating either at the regional master or at another second order center directly controlled by the regional master. The two 5 MHz master buses are fed by PLL-A+B and B+C, respectively. If one of the PLL's fails, both buses remain thus active. Failure of a reference line blocks the frequency control loop. The initial normalized frequency departure from the previous average value is specified to be less than $\pm 2 \cdot 10^{-11}$. Aging and temperature should not cause a departure of more than $5 \cdot 10^{-10}$ after 18 hours of free running. If the frequency control voltage on the oscillator falls below 10% or exceeds 90% of the control range, or if the control loop goes out of lock for other reasons, an alarm signal is activated. The phase differences between the 2048 kHz references and those between the 5 MHz output signals are monitored.

A frequency departure of any output with respect to the two others, exceeding $4 \cdot 10^{-11}$ causes cutoff of the corresponding PLL-unit from the buses and an alarm signal.

In all cases of systematic frequency departure up to $5 \cdot 10^{-5}$, the cutoff must be made before the time interval error of the drifting oscillator reaches 561 ns, in order to remain within the limits of CCITT Rec. G. 811.

The two 5 MHz master buses feed a twin redundant set of synthesizer units generating the output signals required by the multiplexing and switching equipment. The synthesizer units remain the same as in the earlier generation of equipment described in [5].

All important signal voltages and the lock status of the synthesizers are monitored and eventual faults signaled by standard alarm circuits.

The status of the three PLL-units is monitored continuously and compared, allowing unambiguous decision by majority logic decision. This monitoring device also allows detection of multiple faults. In this case, an urgent alarm signal is activated, calling for immediate action in those rare cases of emergency.

The three first order centers controlling a total of about 60 second order centers located in all major nodes of the digital network constitute the backbone of the network timing system. International gateways are always located

at a first or second order center which all are designed to be in compliance with the relevant CCITT G. 800 series recommendations for network synchronization.

3.4 Lower order centers

The third order hierarchical level is constituted by the digital switching systems of the network. Since these systems are provided by several different suppliers, only general input and output signal parameters as well as the jitter transfer properties have been specified. These specifications are to be fulfilled at the interfaces between the transmission and switching systems and are based on the relevant CCITT Recommendations Q. 502, G. 703, G. 742 and G. 811.

The reference signals for the synchronization of the clocks controlling the switching equipment can be supplied in two ways:
a) from the outputs of a second order clock system via additional 2048 kHz clock distribution units.
b) in switching offices where there is no second order clock installed, the switching equipment is synchronized via a minimum of 2 redundant 2048 kbit/s PCM links originating at a second order center.
In case of emergency due to interruption of the reference signal links, the clocks of the switching equipment are allowed to run free at 2048 kHz $\pm$ 50 ppm. Switching of telephone traffic remains possible in this condition, whereas data traffic might be impaired due to increased slip rate. Alarm signals must be activated under such conditions. When the missing reference signals reappear, slave operation must be resumed after 100 ms max. allowed delay. A minimum number of 4 redundant 2048 kHz outputs is required from the switching equipment to drive the clock distribution units feeding the multiplexers of the transmission systems. The jitter transfer specifications, based on CCITT Rec. Q. 502 and others mentioned above, limit the output jitter to levels acceptable to all other connected equipment.

The lowest and fourth level of the timing hierarchy shown in Fig. 1 comprises equipment synchronized by the incoming digital signal such as digital PABX (private automatic branch exchanges) and all kinds of digital terminal equipment. All these devices thus receive their bit timing from the network.

3.5 Planning, building and operational aspects

It is interesting to note that by adhering to rather strict principles of top-down design, it is possible to achieve a high flexibility in planning and installation. The backbone of the network timing system constituted by the first and second order centers in the digital trunk network can grow together with the network itself, since the timing equipment is fully integrated into the transmission network and uses the same equipment standards as the multiplexers and other transmission equipment. In the same way, monitoring and alarm circuits adhere to the same common standards for digital transmission equipment. Operation and maintenance is thus equally integrated and has not caused any particular problems.

4. CONCLUSIONS

The timing concept for the Swiss digital communications network has been developed during the past ten years. It has now matured towards detailed planning and construction. Major parts of the equipment have been operating since 1978. Reliability, performance and serviceability have been within the expected limits. The new master oscillator system design described in an accompanying paper [8], is based on the experience acquired and conforms to the international standards developed during the same period. In this paper, mathematical developments and technical details have been avoided. They can be found in the cited references.

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Note: Many relevant CCITT and CCIR documents are cited in the text. These international Standards are published by the ITU, Geneva, Switzerland. The latest versions of CCITT Recommendations Series G.700 - G.956 are published in the CCITT Red Book, Vol. III, Fasc. III.3, ITU Geneva 1985. The relevant CCIR Recommendations and Reports are published in Vol. VII of the CCIR Books, latest issue 1982, new revisions to be published in 1986.

(●) 1st order center; cesium controlled master

(~) 2nd order center; high stability PLL with digital memory

(⊖) 3rd order centers, switching system clocks

⌄ 4th order centers, PABX and terminal equipment

N1, N2, R3 Reference links
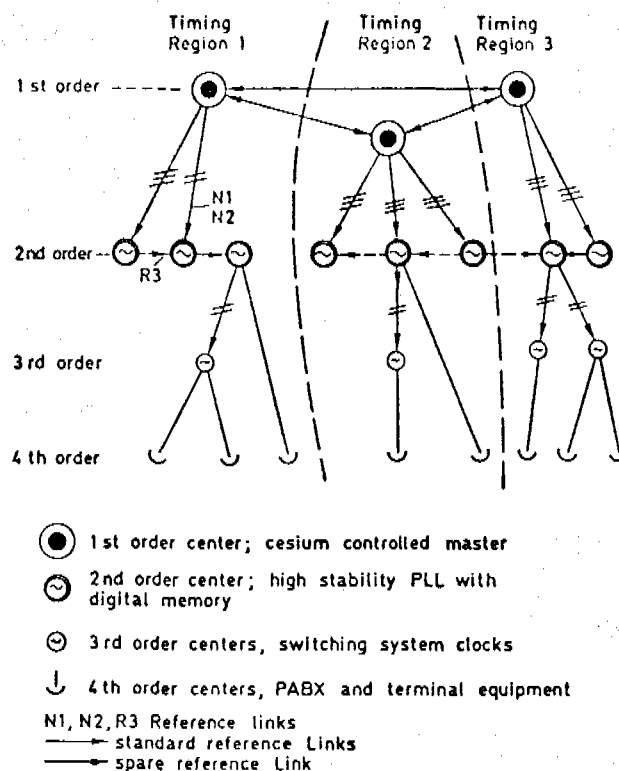—→ standard reference Links
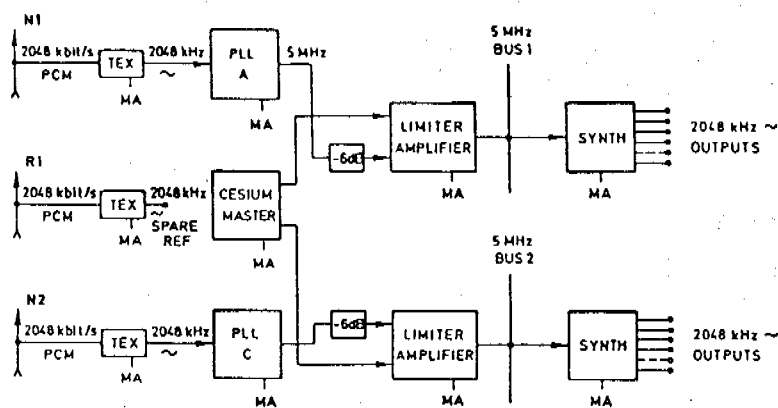——→ spare reference Link

FIG. 1 Timing Network Structure

FIG. 2 First order center
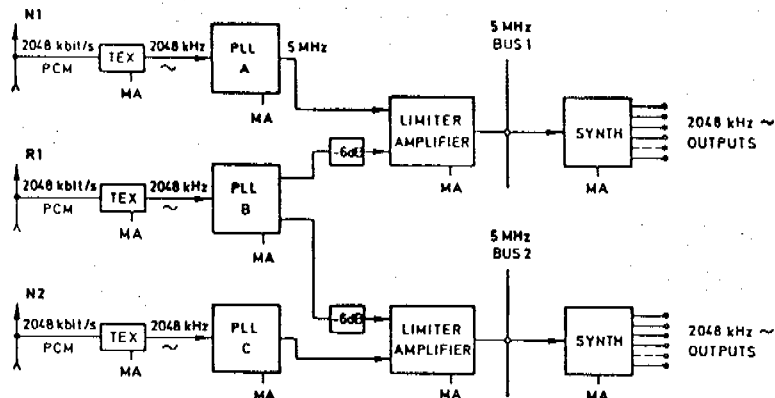MA: connections to monitoring system with majority decision and
alarm circuits (not shown)

FIG. 3 Second order center
MA: connections to monitoring system with majority decision and
alarm circuits (not shown)

QUESTIONS AND ANSWERS

VICTOR REINHARDT, HUGHES AIRCRAFT:
Why did you use the scheme of vectorial addition and hard limiting rather than just selector switches?

MR. KARTASCHOFF:
We don't use the mechanical or PIN switches because of the disappearance of the signal during switching. This way we have no transient of that type.

EDWIN BONDURANT, SATELLITE BUSINESS SYSTEMS:
Your talk was very interesting to me because we run a very similar system in a domestic satellite communication system. We have had an integrated voice and data and video service for several years and we are interested in system synchronization as much as you are. I might just mention that we are running with rubidium standards for a system clock. We are interested in upgrading and would like to chat with you after the session about your experience.

MR. KARTASCHOFF:
We did not use rubidiums because of the simple reason that all of our equipment has the crystals in a good environment, no shock, no vibration. Currently we have operating fourteen cesium Standards for the primaries.